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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,957	10/21/2003	Osamu Ogawa	10873.1316US01	6459

23552 7590 11/19/2004

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,957	OGAWA ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/690957 file on 10/21/03.

Claim 1-15 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada et al. (US Patent 6604232).

3. As to claim 1, Okada et al. teach a high-level synthesis method, comprising: generating a CDFG (Control Data Flow Graph) based on an input file describing a behavior of a digital circuit (see fig 12 abstraction and col5 lines 19-65 and col8 lines 1-5); scheduling the CDFG by allocating each node of the CDFG generated in the CDFG generation, expressing contents of processing, to a time synchronized with a clock called a step, based on the CDFG and a constraint condition of the digital circuit described in a constraint file (see fig 7, 8, fig 12-17 S13 and S14 col 8 lines 4 to col 14 lines 3); generating allocation information representing how resources for constituting the digital circuit are allocated to respective nodes of the CDFG scheduled in the scheduling, based on resource-level layout information representing a layout of the resources, and based on circuit information representing a connecting relationship between

the resources (see fig 7, 8, fig 12-29 S15 col 8 lines 4 to col 14 lines 3); and outputting the circuit information generated in the allocation and circuit information generation (see fig 12-17 and fig 27-29 S15 col 8 lines 10-39 col 14 lines 5-14).

4. As to claim 2, Okada et al. teach wherein the allocation and circuit information generation comprises: generating initial allocation information representing how the resources are allocated to the respective nodes of the CDFG scheduled in the scheduling and initial circuit information representing a connecting relationship between the resources (see fig 27-43 col 12 line 15 to col 18 lines 60); generating the resource-level layout information, based on the initial circuit information generated in the initial allocation and initial circuit information generation (see fig 27-43 col 12 line 15 to col 18 lines 60); generating corrected allocation information representing how an allocation of the resources with respect to the respective nodes of the CDFG is changed and corrected circuit information representing how the connecting relationship between the resources is changed, based on the initial allocation information generated in the initial allocation and initial circuit information generation and the resource-level layout information (see fig 27-43 col 12 line 15 to col 18 lines 60 and summary); and minutely correcting the resource level layout information, based on the corrected circuit information generated in the corrected allocation and corrected circuit information generation, wherein the corrected allocation and corrected circuit information generation, and the resource-level layout minute correction are performed repeatedly until a predetermined standard is satisfied, and in the corrected allocation and corrected circuit information generation, corrected allocation information representing how an allocation of the resources with respect to the respective nodes of the CDFG is changed and corrected circuit information how the connecting relationship

between the resources is changed, are generated based on the resource-level layout information and the corrected allocation information previously generated (see fig 27-43 col 12 line 15 to col 18 lines 60 and summary).

5. As to claim 3, Okada et al. teach wherein the allocation information contains hardware resource allocation information and lifetime information of hardware resources (see col 2 line 14 –31).

6. As to claim 4, Okada et al. teach wherein the resource-level layout information is distance information of arl inter-resource connecting line (see col 2 line 14 to col 4 lines 51).

7. As to claim 5, Okada et al. teach wherein the resource-level layout information is congestion degree information in a layout region of an inter-resource connecting line (see col 2 line 14 to col 4 lines 51).

8. As to claim 6, Okada et al. teach wherein the resource-level layout information is inter-macro connecting line information expressed by any function composed of distance information of an inter-resource connecting line and congestion degree information in a layout region of an inter-resource connecting line (see col 2 line 14 to col 4 lines 51).

9. As to claim 7, Okada et al. teach wherein the resource-level layout information includes a layout influence degree as a coefficient (see col 3 line 1 to col 5 lines 15 background and summary).

10. As to claim 8, Okada et al. teach wherein the resources are allocated to the respective nodes of the CDFG so as to minimize shared hardware resources in the initial allocation and initial circuit information generation, and an allocation of the resources with respect to the respective nodes of the CDFG is changed so that hardware resource separately implemented are

shared in the corrected allocation and corrected circuit information generation (see fig 27-43 col 12 line 15 to col 18 lines 60 and summary and background).

11. As to claim 9, Okada et al. teach wherein the resources are allocated to the respective nodes of the CDFG so as to maximize shared hardware resources in the initial allocation and initial circuit information generation, and shared hardware resources are allocated separately in the corrected allocation and corrected circuit information generation (see fig 27-43 col 12 line 15 to col 18 lines 60 and summary and background).

12. As to claim 10, Okada et al. teach wherein, in the corrected allocation and corrected circuit information generation, an arrangement distribution variation in a layout region of memory resources is calculated, synthesis ease of a synchronization clock circuit is estimated based on the arrangement distribution variation in a layout region of the memory resources, and sharing with high synthesis ease is selected when the memory resources are shared (see fig 12-17 and fig 27-29 S15 col 8 lines 10-39 col 14 lines 5-14 and background).

13. As to claim 11, Okada et al. teach wherein the arrangement distribution variation in the layout region of the memory resources is a variation in number of the memory resources belonging to each region obtained by dividing the layout region into a plurality of regions (see fig 12-17 and fig 27-29 S15 col 8 lines 10-39 col 14 lines 5-14 and summary).

14. As to claim 12, Okada et al. teach wherein the arrangement distribution variation in the layout region of the memory resources is a total of variations calculated for each hierarchy obtained by dividing the layout region hierarchically (see fig 12-17 and fig 27-29 S15 col 8 lines 10-39 col 14 lines 5-14 and summary).

15. As to claim 13, Okada et al. teach wherein the resources are allocated to the respective nodes of the CDFG so as to maximize shared hardware resources in the initial allocation and 11116a1 circuit information generation, the shared hardware resources are separately allocated in the corrected allocation and corrected circuit information generation, and the allocation and circuit information generation further includes changing the allocation by allowing the hardware resources divided in the corrected allocation and corrected circuit information generation to be shared with the hardware resources that are not shared in the initial allocation and initial circuit information generation (see fig 12-17 and fig 27-29 S15 col 8 lines 10-39 col 14 lines 5-14 and summary).

16. As to claim 14, Okada et al. teach wherein the resource-level layout information includes a layout influence degree as a layout influence coefficient, and the corrected allocation and corrected circuit information generation and the allocation changing are repeatedly performed while the layout influence coefficient is corrected in stages (see col 3 line 1 to col 5 lines 15 background and summary).

17. As to claim 15, Okada et al. teach wherein the resource-level layout information minutely corrected in the resource-level layout minute correction is further output in the outputting (see col 3 line 1 to col 5 lines 15 background and summary).

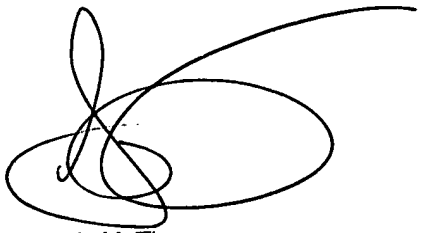
Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
November 13, 2004



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